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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,632	04/24/2006	Guenther Weiss	10191/4152	8448

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EXAMINER	
PIERRE LOUIS, ANDRE	
ART UNIT	PAPER NUMBER
2123	
MAIL DATE	DELIVERY MODE
12/08/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/561,632	WEISS ET AL.	
	Examiner	Art Unit	
	ANDRE PIERRE LOUIS	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-21,23-25 and 27-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-21,23-25 and 27-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 09/15/2008 has received and fully considered.

2. Claims 1-13, 22, and 26 remain cancelled; and claims 27-38 are added.

3. Claims 14-21, 23-25, and 27-38 are now pending and presented for examination.

4. Regarding the rejection under 35 USC 112 2nd paragraph, the Examiner withdraws the rejection in view of the amendment.

5. As per the double patenting rejection, the Examiner acknowledges the receipt of the terminal disclaimer filed on 09/15/2008; the rejection is now withdrawn.

Response to Arguments

6. Applicant's arguments filed 09/15/2008 have been fully considered but they are not persuasive.

6.1 Applicant argues that the Brayton reference does not identically teach the claim features of a plurality of simulation process with corresponding memory modules and interface modules and that Stewart fails to disclose the distinct memory location, the Examiner respectfully disagrees and assert that Brayton et al., used as a primary reference in the rejection of the claims, discloses a system for control system simulation, testing and operator training *(see title), comprises* a plurality of simulation modules 120 of figures 3-4, used to perform a plurality of simulation processes to include the simulation of HMI portion of a control system plant, and simulating the entire control plant *(see for example col.10 lines 14-61).* Brayton et al. continues to substantially disclose the simulation are performed using a plurality of simulation databases/memories where data from the databases are transferred/downloaded and used in testing all function of a PLC *(see col.8 line 63-col.9 line 48).* As clearly stated in the below

rejection, while Brayton et al. does not specifically states that memory modules has distinct memory location, one of ordinary skilled in the art would clearly appreciate the approach taken by Brayton during his simulating and testing of the control system, as Brayton discloses downloading simulation data from one place to another. But, Stewart, used a secondary reference in the rejection of the claims does provides of a Design of Dynamically Reconfigurable Real-Time software Using Port-Based Objects, including facilitating communication of inter-modules via distributed/assigned and distinct memory locations *(see fig.6, section 4 , page 761, 766-768).*

6.2 The Examiner realizes that Applicant does not address the secondary rejection shown below and therefore provides no response to the secondary rejection.

6.3 While the applicants believe that the independent claims along with their dependencies should be found allowable, the Examiner respectfully disagrees and asserts that the combined references cited teach the entire claimed invention, as evidenced by the new grounds of rejection set forth below. The Examiner further asserts that the response to arguments along with the rejection below clearly support the Examiner's position in the rejection of the instant claims. *However, the Examiner highly encourages the Applicant to take a look at the additional references cited not used located in the conclusion section of this and the previous office action.*

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7.0 Claims 14-21, 23-25, and 27-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brayton et al. (U.S. Patent No. 6,823,280), in view of Stewart et al. (Design of Dynamically Reconfigurable Real-Time software Using Port-Based Objects, 12/1997).

7.1 In considering claims 14, 21, 25, Brayton et al. discloses a computer implemented method for simulation and verification of a control system under development, comprising: an arrangement for performing a plurality of simulation and verification of a control system processes with corresponding memory modules and interface modules, wherein the memory modules include distinct memory locations for inter-module communication, and the system modules are dynamically reconfigured with each other *(fig.3-4, col.4 lines 18-62, col.5 lines 14-62; also see col. 8 line 63-col.9 line 48).* Although Brayton et al. does not specifically states that memory modules has distinct memory location, one of ordinary skilled in the art would clearly appreciate the approach taken by Brayton during his simulating and testing of the control system. Nevertheless, Stewart substantially teaches Design of Dynamically Reconfigurable Real-Time software Using Port-Based Objects, including facilitating communication of inter-modules via distinct memory locations *(see for example fig.6 page 766-768 (section 4)).* Brayton et al. and Stewart are analogous art because they from the same field of endeavor and that the design analyzes by Stewart is similar to that of Brayton et al. Therefore it would have been obvious to

one of ordinary skilled in the art to combine the system of Stewart with the simulation method and system of Brayton et al. because Stewart teaches the advantage of performing maintenance on the fly and real-time system implementation using time-based decomposition *(see section 2.1)*.

7.2 Regarding claims 15, 27, and 35, the combined teachings of Brayton et al. and Stewart substantially teach that the simulation is performed by running a control system simulation model, the simulation model including a number of sub-models being performed on one of the plurality of system modules, respectively *(see Brayton fig.4, col.4 lines 18-62)*.

7.3 As per claims 16, 23, 28, and 36, the combined teachings of Brayton et al. and Stewart substantially teach that at least some of the system modules are dynamically reconfigurable for communication via distinct memory locations *(see Brayton et al. fig.3-4, col.5 lines 14-62, and col.6 line 58-col.7 line 10; also see Stewart pgs. 766-768)*.

7.4 With regards to claims 17, 29, and 37, the combined teachings of Brayton et al. and Stewart substantially teach the cross-bar switch for dynamic configuration of the distinct memory locations *(see Brayton et al. fig.3-4, col.6 line 58-col.7 line 40; also see col.10 lines 24-61)*.

7.5 Regarding claim 18, the combined teachings of Brayton et al. and Stewart substantially teach that the interconnection scheme for coordination of the distinct memory locations *(see Brayton et al. fig.4, col.4 lines 18-62, col.10 lines 24-61; also see Stewart pages 761-768)*.

7.6 As per claims 19 and 30, the combined teachings of Brayton et al. and Stewart substantially teach the host-target communication interface for connection of the simulation

system with a simulation host, an input interface, and output interface *(see Brayton et al. col.1 lines 16-67; also see fig.4 col.3 line 1-col.4 line 62; also Stewart pgs.761-765).*

7.7 With regards to claims 20, 24, and 31, the combined teachings of Brayton et al. and Stewart substantially teach that the modules includes at least one output port server for communication interconnection with respective output service of the other modules *(see Brayton et al. fig.1-2, col.4 lines 18-62; also see Stewart pgs.761-762).*

7.8 With regards to claim 32, the combined teachings of Brayton et al. and Stewart substantially teach that wherein dynamic reconfiguration of the distinct memory locations is achieved according to an interconnection scheme, and wherein inter-module communication is achieved via output port service of the various modules *(see Brayton et al. fig.4, col.4 lines 18-62, col.10 lines 24-61; also see Stewart pages 761-768).*

7.9 As per claim 33, the combined teachings of Brayton et al. and Stewart substantially teach that wherein a simulation is performed by running a control system simulation model, the simulation model including a number of sub- models being performed on one of the plurality of system modules, respectively, wherein at least two of the system modules are dynamically reconfigurable for communication via distinct memory locations, and wherein there is a cross-bar switch for dynamic configuration of the distinct memory locations, and wherein the cross-bar switch comprises an interconnection scheme for coordination of the distinct memory locations *(see Brayton et al. col.1 lines 16-67; also see fig.4 col.3 line 1-col.4 line 62; also Stewart pgs.761-768).*

7.10 Regarding claims 34 and 38, the combined teachings of Brayton et al. and Stewart substantially teach that wherein there is a host-target communication interface for

connection of the simulation system with a simulation host, an input interface, and an output interface, wherein the modules include at least one output port server for communication interconnection with respective output port service of other modules, and wherein dynamic reconfiguration of the distinct memory locations is achieved according to an interconnection scheme, and wherein inter-module communication is achieved via output port service of the various modules *(see Brayton et al. col.1 lines 16-67; also see fig.4 col.3 line 1-col.4 line 62; also Stewart pgs.761-768)*.

8. Claims 14-21, 23-25, 27-38 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (refer to herein as AAPA)), in view of Stewart et al. (Design of Dynamically Reconfigurable Real-Time software Using Port-Based Objects, 12/1997)..

8.1 In considering claims 14, 21, 25, AAPA substantially teaches a computer implemented method for simulation and verification of a control system under development, comprising: an arrangement for performing a plurality of simulation and verification of a control system processes with corresponding memory modules and interface modules, wherein the memory modules include distinct memory locations for inter-module communication, and the system modules are dynamically reconfigured with each other *(see fig.1-2, also applicant's background)*. However, AAPA does not specifically state that the memory modules have distinct memory location; but Stewart substantially teaches Design of Dynamically Reconfigurable Real-Time software Using Port-Based Objects, including facilitating communication of inter-modules via distinct memory locations *(see for example page 766-768 (section 4))*. Therefore it would have been obvious to one of ordinary skilled in the art to combine the system of Stewart with the

AAPA because Stewart teaches the advantage of performing maintenance on the fly and real-time system implementation using time-based decomposition *(see section 2.1)*.

8.2 Regarding claims 15, 27, and 35, the combined teachings of AAPA and Stewart substantially teach that the simulation is performed by running a control system simulation model, the simulation model including a number of sub-models being performed on one of the plurality of system modules, respectively *(see AAPA fig. 1-2, also see Stewart page 760-768)*.

8.3 As per claims 16, 23, 28, and 36, the combined teachings of AAPA and Stewart substantially teach that at least some of the system modules are dynamically reconfigurable for communication via distinct memory locations *(see Stewart pgs. 766-768)*.

8.4 With regards to claims 17, 29, and 37, the combined teachings of AAPA and Stewart substantially teach the cross-bar switch for dynamic configuration of the distinct memory locations *(see Stewart pages 760-768)*.

8.5 Regarding claim 18, the combined teachings of AAPA and Stewart substantially teach that the interconnection schemes for coordination of the distinct memory locations (see *AAPA fig.1-2; also see Stewart pages 761-768)*.

8.6 As per claims 19 and 30, the combined teachings of AAPA and Stewart substantially teach that the host-target communication interface for connection of the simulation system with a simulation host, an input interface, and output interface *(see pgs.761-765)*.

8.7 With regards to claims 20, 24, and 31, the combined teachings of AAPA and Stewart substantially teach that the modules includes at least one output port server for communication interconnection with respective output service of the other modules *(see Stewart pgs.761-762)*.

8.8 With regards to claim *32, the* combined teachings of AAPA and Stewart substantially teach that wherein dynamic reconfiguration of the distinct memory locations is achieved according to an interconnection scheme, and wherein inter-module communication is achieved via output port service of the various modules (see *AAPA fig.1-2; also see Stewart pages 761-768).*

8.9 As per claim *33,* the combined teachings of AAPA and Stewart substantially teach that wherein a simulation is performed by running a control system simulation model, the simulation model including a number of sub- models being performed on one of the plurality of system modules, respectively, wherein at least two of the system modules are dynamically reconfigurable for communication via distinct memory locations, and wherein there is a cross-bar switch for dynamic configuration of the distinct memory locations, and wherein the cross-bar switch comprises an interconnection scheme for coordination of the distinct memory locations *(see AAPA fig.1-2; also see Stewart pages 761-768).*

8.10 Regarding claims *34 and 38,* the combined teachings of AAPA and Stewart substantially teach that wherein there is a host-target communication interface for connection of the simulation system with a simulation host, an input interface, and an output interface, wherein the modules include at least one output port server for communication interconnection with respective output port service of other modules, and wherein dynamic reconfiguration of the distinct memory locations is achieved according to an interconnection scheme, and wherein inter-module communication is achieved via output port service of the various modules *(see AAPA fig.1-2; also see Stewart pages 761-768).*

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9.1 Nam et al. (USPG_PUB No. 2005/0018803) teaches a control rod driving simulator for verification of control system rod driving mechanism control system of atom power plant.

10. Claims 1-13, 22, and 26 remain cancelled and claims 14-21, 23-25, and 27-38 are rejected and **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. P. L/
Examiner, Art Unit 2123

December 2, 2008

/Paul L Rodriguez/
Supervisory Patent Examiner, Art Unit 2123